--REMARKS--

The present reply is in response to a Final Office Action, dated September 26, 2002. Claims 14-26 are currently pending in the present application.

In the Final Office Action, Examiner Ellis rejected pending claims 14-26 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 4,454,578 to *Masumoto* et al. The Applicant has thoroughly considered Examiner Ellis' remarks concerning the patentability of independent claims 14, 20 and 21over *Matsumoto*. The Applicant has also thoroughly read *Matsumoto*.

To warrant this §102(b) rejection, *Matsumoto* must show each and every limitation of independent claims 14, 20 and 21 in as complete detail as in contained in independent claims 14, 20 and 21. See, MPEP §2131. The Applicant respectfully traverses this §102(b) rejection of independent claims 14, 20 and 21, because *Matsumoto* fails, among other things, to disclose, teach or suggest "an expansion bit indicative of whether the processing system expands the first set of data value bits or reads any additional parameter bytes including additional sets of data value bits" as recited in independent claim 14, and "a second indicator representative of whether to expand the plurality of data value bits" as recited in dependent claim 22.

Specifically, Examiner Ellis interprets the operand specifier illustrated in FIG. 2a of *Matsumoto* as having an expansion bit 00 for a LIT field of data value bits. *Matsumoto* actually discloses the operand specifier of FIG. 2a having bits 00 to indicate the LIT field of data value bits is no longer than five bits. See, *Matsumoto* at column 3, line 66 to column 4, line 3. At best, the bits 00 of the operand specifier of FIG. 2a are representative of a number of data value bits or a number of bytes in the operand specifier of FIG. 2a. As such, the first indicators recited in independent claims 20 and 21 are arguably disclosed by *Matsumoto*. However, contrary to the assertion by Examiner Ellis, *Matsumoto* clearly does not disclose, teach or suggest an expansion bit or a second indicator as claimed in independent claim 14 and dependent claim 22, respectively.

Moreover, the objective of *Matsumoto* is to provide a technique for handling instructions having a fixed operation code and a variable length operand specificer (e.g., the operand specifiers illustrated in FIGS. 1a-3F). To this end, *Matsumoto* teaches away from an expansion of data value bits in the operand specifier by exclusively teaching an instruction fetch unit 400 that properly aligns the data value bits of the operand specifier bit by bit via a shifting of the data value bits. Upon completion of the shifting, the aligned data value bits are immediately passed to an instruction decode unit 500 without expansion or insertion of any additional data value bits. See, *Matsumoto* at column 4, lines 56-65.

The Applicant has cancelled dependent claim 22, and amended independent claims 20 and 21 to include the limitation of cancelled claim 22. Withdrawal of the rejection of claims 14, 20, 21 and 22 under 35 U.S.C. §102(b) as being anticipated by *Matsumoto* is therefore respectfully requested.

Claims 15-19 depend from independent claim 1. Therefore, dependent claims 15-19 include all of the elements and limitations of independent claim 14. It is therefore respectfully submitted by the Applicants that dependent claims 15-19 are allowable over *Matsumoto* for at least the same reason as set forth above with respect to independent claim 14.

Claims 23-26 depend from independent claim 20. Therefore, dependent claims 23-26 include all of the elements and limitations of independent claim 20. It is therefore respectfully submitted by the Applicants that dependent claims 23-26 are allowable over *Matsumoto* for at least the same reason as set forth above with respect to independent claim 20.

Claims 23-26 also depend from independent claim 21. Therefore, dependent claims 23-26 include all of the elements and limitations of independent claim 21. It is therefore respectfully submitted by the Applicants that dependent claims 23-26 are allowable over *Matsumoto* for at least the same reason as set forth above with respect to independent claim 21.

Withdrawal of the rejection of dependent claims 15-19 and 23-26 under 35 U.S.C. §102(b) as being anticipated by *Matsumoto* is therefore respectfully requested.

SUMMARY

Examiner Ellis' 35 U.S.C. §102(b) rejection of claims 14-26 has been obviated by above remarks concerning the patentability of independent claim 14 over *Matsumoto*, the amendments and remarks concerning the patentability of amended independent claims 20 and 21 over *Matsumoto*, and the cancellation of dependent claim 22. The Applicant respectfully submits that claims 14-21 and 23-26 as added herein fully satisfy the requirements of 35 U.S.C. §§ 102, 103 and 112. In view of the foregoing, favorable consideration and early passage to issue of the present application is respectfully requested.

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

20. (Amended) A method of forming instructions for execution in a processing system, said method comprising:

providing an opcode portion determining at least one instruction to be performed by the processing system; and

providing a parameter portion including a plurality of data value bits, [and] a first indicator representative of a number of the plurality of data value bits, and a second indicator representative of whether to expand the plurality of data value bits.

21. (Amended) A method of forming instructions for execution in a processing system, said method comprising:

providing an opcode portion determining at least one instruction to be performed by the processing system; and

providing a parameter portion including a plurality of data value bits, [and] a first indicator representative a number of bytes in the parameter portion, and a second indicator representative of whether to expand the plurality of data value bits.